Proceedings: ***International Invention, Innovative & Creative (InIIC) Conference, Series 1/2021***
eISBN: 978-967-18412-5-9 (Publication Date: 30 June 2021) *MNNF Publisher*

Study on Copper Pillar Bump in Flip Chip Technology using Computational Fluid Dynamics

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ABSTRACT
In flip-chip technology, the solder bump flip-chip bonding is the most common bonding used to provide electrical connections and mechanical supports to the assembly. However, due to the rising demand from the emerging market economies, there is a growing need for fine pitch flip-chip technology to fulfill the future demands. This is because the electronic devices which are thin, fast, light, and powerful are more preferable in the electronic market. The demand for smaller chip and interconnection joints causes the bottleneck of the conventional flip-chip technology. Therefore, a copper (Cu) pillar bump with a solder cap which can offer numerous advantages over the conventional solder bump is proposed to replace it. In this study, the conventional solder bump and Cu pillar bump models are developed to investigate their differences using the Computational Fluid Dynamics (CFD). Both the solder and Cu pillar bumps are modelled in ANSYS Fluent software, and the temperature distributions during the solder reflowing process are simulated. The simulation results indicate that the heat transfer of assembly with interconnections of Cu pillar bumps in the reflow oven is better than conventional solder bumps.

Key Words: Flip Technology, Reflow soldering, Copper Pillar Bump, Surface Mount Technology, Computational Fluid Dynamics

1. INTRODUCTION

Electronic packaging is the methodology for connecting and interfacing the chip technology with a system and the physical world (Datta, 2019). Based on Tsai et al. (2017), flip-chip technology is one of the chip-package interconnection techniques that uses solder bumps to connect the die to the package carrier such as substrate electrically.

Due to the future trends towards smaller, lighter, cheaper and faster electronic devices, the conventional flip-chip technology has reached its bottleneck. Figure 1 clearly shows that the future trend of interconnection joints towards smaller and thinner as well as the bump pitch size is reduced below 150µm. Hence, the copper (Cu) pillar technology which can fulfil all the demands, has been suggested in the electronic industry. The Cu pillar with a solder cap offers superior electrical and thermal properties (Henderson, 2012), and it can get finer pitch with providing better electromigration performance and being more compatible with the bump-on-trace (BOT) process (Long et al., 2020).

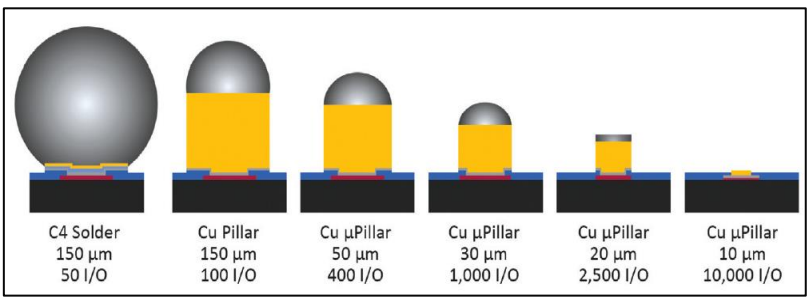

Figure 1: Flip Chip Interconnect Bumping from C4 Solder to Direct Cu (Gregorich & Gu, 2019)

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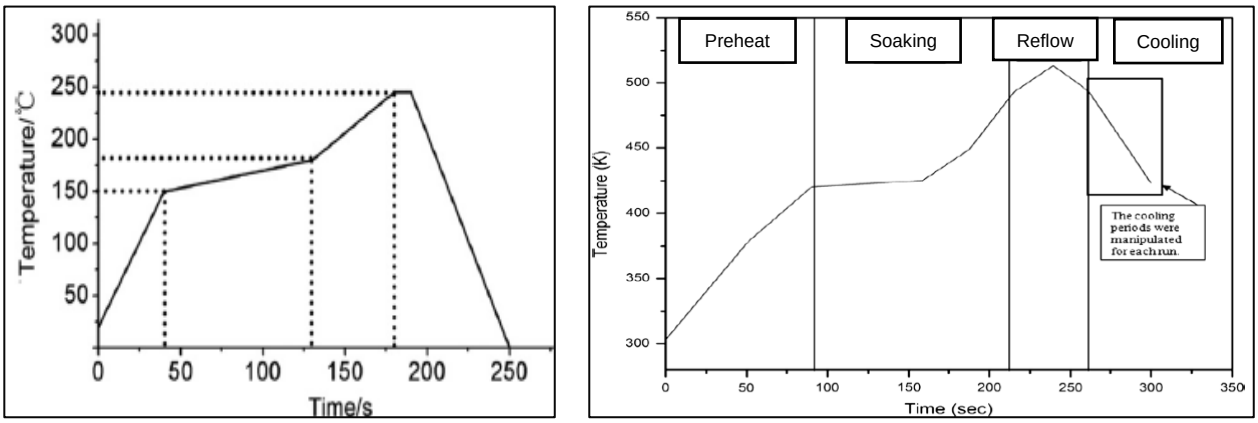
Generally, Surface Mounted Technology (SMT) processes start with the solder paste printing process, then continues with the component mounting process. The solder paste is dissipated on a substrate using a stencil and the electrical components are placed on the substrate. Lastly, the assembly is sent to a reflow oven to undergo the reflow soldering process (Rusdi et al., 2018; Asghar et al., 2020). In the oven, the assembly is travelled into different heating zones, namely preheating, soaking, reflow and cooling stages.

Soldering is a method of producing a permanent mechanical and electrical connection between metals by chemically reacting with other metals (Thakur et al.,2015). Due to health concerns and environmental issues, the use of lead-free solder paste is preferable compared to lead-based solder paste (Srivalli et al., 2015). According to Rusdi et al. (2019), the most commonly used solder paste material is SAC solder paster which is lead-free and consists of Tin (Sn), Silver (Ag) and Copper (Cu).

Based on Tao et al. (2017), the temperature profile of the SMT Scope is a standard lead-free temperature profile for SAC305. As shown in Figure 2(a), the reflow stage occurs between the time 125 to 185s approximately, and the peak temperature is 245°C. Srivalli et al. (2015) stated that the reflow oven is set according to the valid temperature zones as shown in Figure 2(b), where the reflow time range is between 220s to 280s.



a) b)

Figure 2: Temperature Profile of The Reflow Process: (a) Tao et al. (2017), (b) Srivalli et al. (2015)

There are numerous numerical approaches that can be used to simulate the reflow soldering process, including Finite Element Method (FEM) and Finite Volume Method (FVM). The recent findings from different researchers have been tabulated in Table 1. Based on the previous findings, it is clear that the majorities of the studies which are done on Cu pillar bump are FEM and limited to stress analysis. Through numerical simulation, the thermal behaviour of interconnection joints can be simulated and used to predict the solder joint defects such as void formation and crack propagation. This is important as the numerical simulation is a cost-effective and time-saving tool that helps to improve the reflow process.Thus, in this paper, both the solder bump and Cu pillar bump are compared, and their reflow oven temperature distributions during reflow soldering are simulated using ANSYS Fluent.

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Table 1: Previous Findings

Authors	Numerical Approaches	Interconnection Joints	Findings
Najib et al. (2015)	FVM	Solder bump	Air circulation mechanism in reflow oven was demonstrated and validated with experiment results.
Srivalli et al. (2015)	FVM	Solder bump	The thermal behaviour of solder joint at different cooling durations was simulated and compared with experiment.
Deng et al. (2016)	FEM	Solder bump	The temperature distribution of sistem-in-package (SiP) assembly in an oven was simulated to design a thermal profile with minimal temperature gradients.
Esfandyari et al. (2017)	FEM	Solder bump	The thermal behaviour of solder joint was predicted and the simulation data has a good conformity with experiment.
Tang et. al (2018)	FEM	Solder bump	The temperature zones in the reflow oven was simulated. After various temperature zones, the temperature distribution was uneven.
Chen et. al (2014)	FEM	Cu pillar bump with solder cap	Stress simulation was conducted and stress distribution of the Cu pillar bump was predicted to investigate the crack formation.
Che et. al (2014)	FEM	Cu pillar bump with solder cap	
Ma et. al (2016)	FEM	Cu pillar bump with solder cap	
Long et. al (2020)	FEM	Cu pillar bump with solder cap	
Sun et. al (2020)	FEM	Cu pillar bump with solder cap	

2. METHODOLOGY

The methodology developed in this study is used for predicting the temperature distribution in an oven, and the simulation process is shown in Figure 3. The basic idea is to set up a new method to analyse the difference between the interconnection using solder joints and Cu pillar bumps inside the oven using ANSYS Fluent, which is a FVM-based software. Figure 4 illustrates the schematic diagrams of the model, consisting of an oven, a ball grid array (BGA) chip, a substrate and solder joints or copper pillar bumps. Two models are developed based on the currently known requirements shown in Table 2.

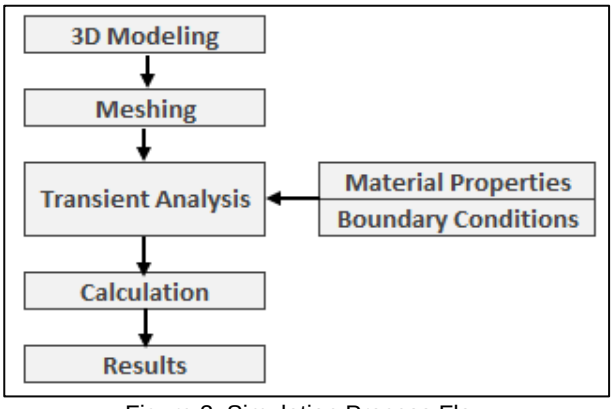

Figure 3: Simulation Process Flow

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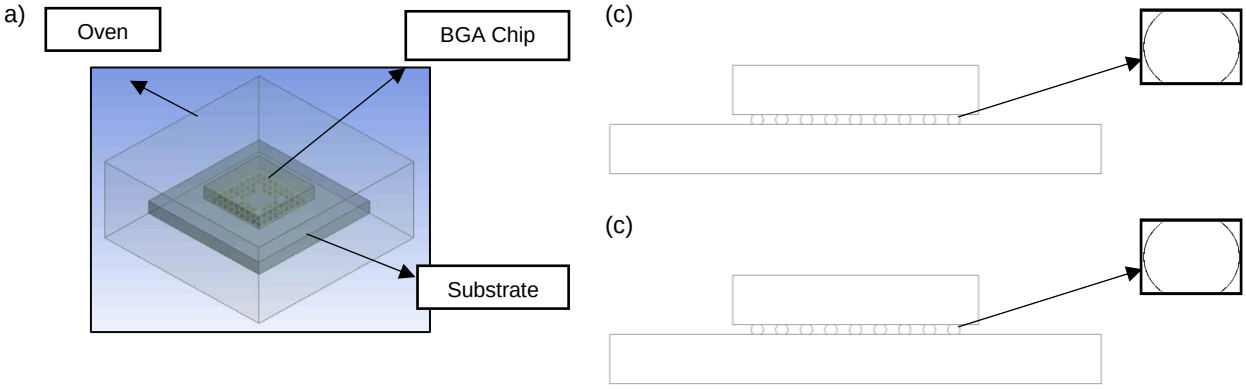

Figure 4: Schematic Diagrams of Model: (a) Isometric View of Model, (b) Simplified Copper Pillar Bump with Solder Cap Model, (c) Simplified Solder Bump Model

Table 2: Dimension of Models

Material	Dimension (mm)
BGA Chip	5 x 5 x 1
Copper Pillar with Solder Cap	Height: 0.1
	Diameter: 0.25
SAC305 Solder	Height: 0.1
	Diameter: 0.25
Substrate (Copper Pad)	10 x 10 x 1
Oven	16 x 16 x 8.1

After building the 3D model, meshing is done as shown in Figure 5, body sizing is applied on the oven body and face sizing is applied on the other electrical components. Then, transient analysis is conducted by setting up the material properties of oven and electrical components, as well as the boundary conditions. The heated wall in the oven is set as discrete ordinations (DO) radiation model and user-defined function (UDF) is created for the reflow soldering process. The UDF is interpreted in Ansys Fluent software and it changes according to different durations at the reflow soldering stage. A simulation for the time period from t = 0 to t = 300s is run, the number of the time step is set as 30,000 and the time step size is set as 0.01 before running the simulation.

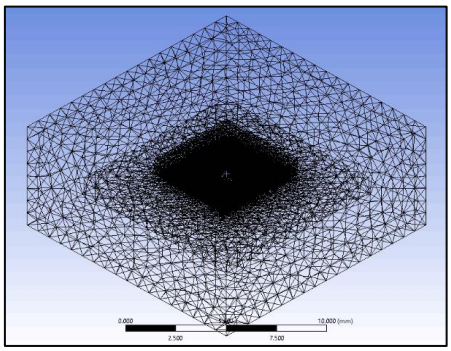

Figure 5: Model Meshing

3. RESULTS & DISCUSSION

In the process, the heat is transferred to the substrate with BGA assembly from a heated wall. In the heat transfer, the interconnection joints like solder joint or copper pillar bump with solder cap slowly absorb the heat from the substrate and start to melt according to the thermal profile setting (Srivalli et al., 2015). The amounts of heat distributed throughout the interconnection joints at different durations of the reflow stage are obtained from the numerical simulation. Figure 6 shows the temperature distribution contour comparison of conventional solder bump and copper pillar bump with solder cap at different durations of the reflow soldering process.

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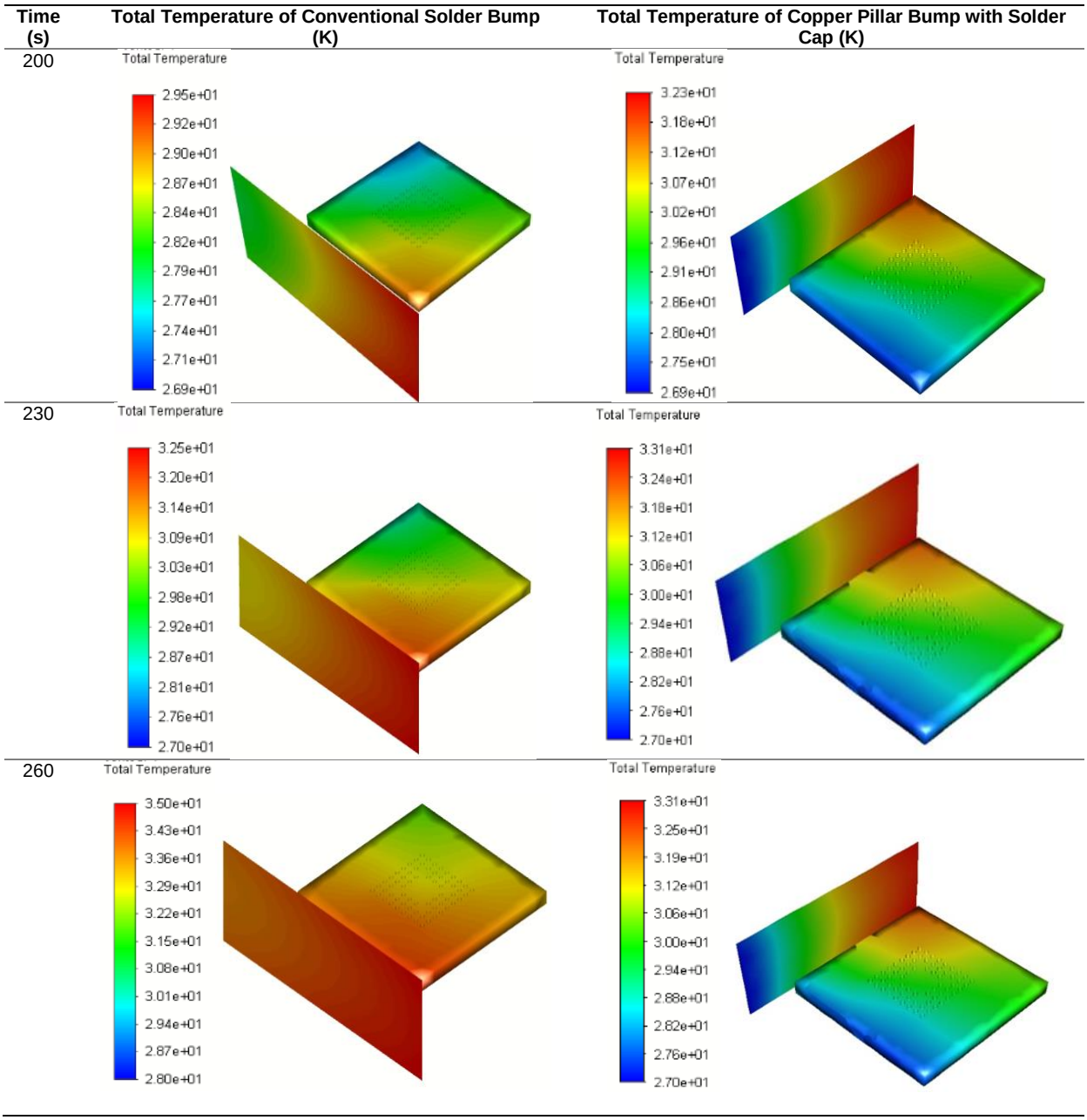

Figure 6: Temperature Distribution Contour Plot of Models (Isometric View)

The highest and lowest temperatures of both convention solder bump and Cu pillar bump at 200s, 230s and 260s have been tabulated in Table 2. Also, the temperature differences between them have been calculated and recorded in the Table 3.

Table 3: Deviation of Highest and Lowest Temperature

	Conventional Solder Bump			Copper Pillar with Solder Cap		
Time (s)	200	230	260	200	230	260
Highest Temperature (K)	29.5	32.5	35.0	32.3	33.1	33.1
Lowest Temperature (K)	26.9	27.0	28.0	26.9	27.0	27.0
Deviation (K)	2.6	5.5	7.0	5.4	6.1	6.1

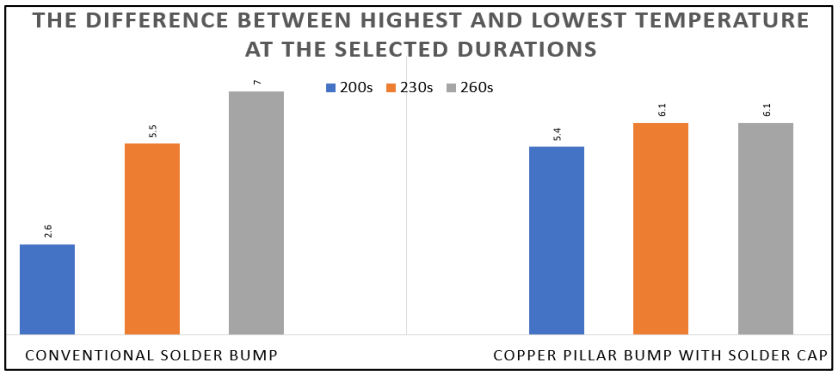

Figure 7: Graph of Temperature Difference

Based on Figure 7 which compares the temperature difference between solder bump and Cu pillar, it can be concluded that the heat transfer through the conventional solder bump is not consistent, thus resulting in the variation of temperature distribution. The inconsistency in the temperature distribution of conventional solder bump has been proven by Tang et al.(2015). The simulation results showed that the temperature distribution of solder joints is not uniformly distributed after various temperature zones.

Therefore, it can be concluded that the small difference in the temperature gradient, showing that the whole model is heated up evenly and this reduces the possibility of the interconnection joint failure. Besides that, the model will spend less time in the oven and thus saving cost and fuel as well as improve the quality of the solder joint.

4. CONCLUSION & RECOMMENDATION

As a result, this simulation highlights the correlations of temperature distributions between both conventional solder bump and copper pillar with solder cap at different reflow soldering periods. The results reveal that copper pillar bump with solder cap performs better than the conventional solder bump as it offers smaller deviation of temperature distributions at the selected periods.

In terms of improving simulation result, grid independent test on the meshing elements of the simulation model is needed to check the consistency of temperature distribution and choose the most optimum case which is able to reduce the computational cost. The structure of the package assembly is symmetric, it is suggested to slice the assembly into half diagonally so that the computational time can be reduced.

Also, the reliability of the interconnection joint can be tested and performed by different methods such as shear test, pull test and thermal shock test. Besides, the execution of the experiment is also important and required to validate the results generated from the virtual simulation. From the experiment, visual inspection with the help of electronic microscope can be used to examine the interconnection joints and their possible defects.

ACKNOWLEDGEMENT

The work is financially supported by Ministry of Higher Education under Fundamental Research Grant Scheme, FRGS (203/PMEKANIK/6071489). The authors would also like to thank Universiti Sains Malaysia for providing technical support.

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